II. AMENDMENTS TO THE CLAIMS

The following is a courtesy copy of the currently pending claims; no revisions have been made via this document:

1. (Previously Presented) A system for positioning I/O pads on a chip, comprising:

an information access system for accessing a control file that includes a proposed placement of a set of I/O pad groups on the chip, wherein each of the set of I/O pad groups includes at least one power pad;

a calculation system for calculating a group switching current of a particular I/O pad group identified in the control file based on individual switching currents of each I/O pad in the particular I/O pad group, and for comparing the group switching current to a predetermined maximum switching current; and

a corrective action system for implementing a corrective action if the group switching current exceeds the predetermined maximum switching current.

2. (Original) The system of claim 1, wherein the corrective action system relocates at least one I/O pad in the particular I/O pad group to another I/O pad group if the group switching current exceeds the predetermined maximum switching current.

3. (Previously Presented) The system of claim 1, wherein each of the set of I/O pad groups includes one power pad.

4. (Original) The system of claim 3, wherein the corrective action system inserts an additional power pad into the particular I/O pad group if the group switching current exceeds the predetermined maximum switching current.

5. (Original) The system of claim 1, wherein the individual switching currents are determined from an I/O limit table, and wherein the maximum switching current is determined from an information file.

6. (Original) The system of claim 1, wherein the chip is a peripheral wire bond chip.

7. (Original) The system of claim 1, further comprising an error detection system for detecting and reporting errors in the control file.

8. (Previously Presented) A computer-implemented method for positioning I/O pads on a chip, comprising:

providing a control file that includes a proposed placement of a set of I/O pad groups on the chip, wherein each of the set of I/O pad groups includes at least one power pad;

calculating a group switching current of a particular I/O pad group identified in the control file based on individual switching currents of each I/O pad in the particular I/O pad group;

comparing the group switching current to a predetermined maximum switching current; and

implementing a corrective action if the group switching current exceeds the predetermined maximum switching current.

9. (Original) The method of claim 8, wherein the calculating step comprises calculating a group switching current of a particular I/O pad group identified in the control file by summing individual switching currents of each I/O pad in the particular I/O pad group.

10. (Original) The method of claim 8, wherein the implementing step comprises relocating at least one I/O pad in the particular I/O pad group to another I/O pad group if the group switching current exceeds the predetermined maximum switching current.

11. (Previously Presented) The method of claim 8, wherein each of the set of I/O pad groups includes one power pad.

12. (Original) The method of claim 11, wherein the implementing step comprises inserting an additional power pad into the particular I/O pad group if the group switching current exceeds the predetermined maximum switching current.

13. (Original) The method of claim 8, wherein the individual switching currents are determined from an I/O limit table, and wherein the maximum switching current is determined from an information file.

14. (Original) The method of claim 8, further comprising:

detecting errors in the control file; and

reporting the errors.

15. (Original) The method of claim 8, wherein the chip is a peripheral wire bond chip.

16. (Previously Presented) A program product stored on a recordable medium for positioning I/O pads on a chip, which when executed comprises:

program code for accessing a control file that includes a proposed placement of a set of I/O pad groups on the chip, wherein each of the set of I/O pad groups includes at least one power pad;

program code for calculating a group switching current of a particular I/O pad group identified in the control file based on individual switching currents of each I/O pad in the particular I/O pad group, and for comparing the group switching current to a predetermined maximum switching current; and

program code for implementing a corrective action if the group switching current exceeds the predetermined maximum switching current.

17. (Original) The program product of claim 16, wherein the program code for implementing a corrective action relocates at least one I/O pad in the particular I/O pad group to another I/O pad group if the group switching current exceeds the predetermined maximum switching current.

18. (Previously Presented) The program product of claim 16, wherein each of the set of I/O pad groups includes one power pad.

19. (Original) The program product of claim 18, wherein the program code for implementing a corrective action inserts an additional power pad into the particular I/O pad group if the group switching current exceeds the predetermined maximum switching current.

20. (Original) The program product of claim 16, wherein the individual switching currents are determined from an I/O limit table, and wherein the maximum switching current is determined from an information file.

21. (Original) The program product of claim 16, further comprising program code for detecting and reporting errors in the control file.

22. (Original) The program product of claim 16, wherein the chip is a peripheral wire bond chip.